

REMARKS

Applicants respectfully request favorable reconsideration of this application, as amended.

By this Amendment, Claims 1, 4-7, 9, 10, 12, 14, 15, 21, 24, 25, 27, and 28 have been amended; Claims 13 and 18 have been cancelled without prejudice or disclaimer; and Claim 79 has been added. Claims 11, 19, 20, 22, 23, 26, and 29-78 were previously cancelled without prejudice of disclaimer. Accordingly, Claims 1-10, 12, 14-17, 21, 24, 25, 27, and 28 are pending, with Claim 1 being the sole independent claim.

Without acceding to the rejections under 35 U.S.C. § 112, Applicants have cancelled Claims 13 and 18, as noted above, and amended Claims 10, 12, and 14 to overcome the rejections. Withdrawal of the rejections is respectfully requested.

The double patenting rejection is not understood, as Applicants cannot ascertain from the Office Action whether the Examiner intended to rely upon the cited patents individually or was proposing to combine them (which would of course be improper). Moreover, the rejection did not attempt to indicate any specific correspondence between the elements of Applicants' claims and those of the cited patents. If the Examiner should determine to maintain the

rejection with respect to the claims as amended herein, Applicants would appreciate appropriate elaboration of the rationale for such rejection.

Without concession as to propriety of the rejection based on Hiraki, Applicants have amended independent Claim 1 to clarify the invention intended to be claimed. Claim 1 now more particularly recites, *inter alia*, a dynamic random access memory interface to outside the memory module for accessing the dynamic random access memory from outside the memory module, and a static random access memory interface to outside the memory module for accessing the static random access memory from outside the memory module. It is apparent that Hiraki fails to teach or suggest these features of Claim 1.

The Office Action evidently equates data terminals Hiraki's register means located inside respective nonvolatile and volatile memories to the claimed dynamic random access memory interface and the static random access memory interface, respectively. See Office Action at 5. However, even assuming *arguendo* that the data terminals of Hiraki can properly be regarded as interfaces, they clearly would not constitute interfaces to the outside, in contrast to the interfaces set forth in Claim 1. Rather, they provide memory connections to an inner bus.

Applicants also note that Hiraki discloses an input/output circuit 14, which is provided with an input/output port, a bus controller, and an input/output peripheral circuit represented by a serial interface circuit, and which is connected with an external address bus 18A, an external data bus 18D, an external control bus 18C. See Hiraki, col. 10, lines 16-24. The single input/output circuit of Hiraki, however, does not constitute a teaching or suggestion of two memory interfaces - namely, a dynamic random access memory interface and a static random access memory interface, as claimed.

In view of the aforementioned deficiencies of Hiraki with respect to Applicants' invention, at least as presently claimed, Claim 1 clearly distinguishes patentably from the reference.

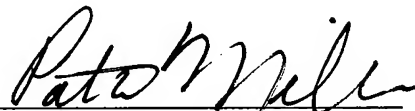
Furthermore, Tanzawa, which was used as a secondary reference to reject Claims 16 and 17 under 35 U.S.C. § 103(a), also fails to teach or suggest the above features of Claim 1.

Accordingly, it is respectfully urged that the outstanding rejections be withdrawn and that this application now be passed to issue.

Applicants respectfully solicit an early Notice of Allowance.

The Commissioner is hereby authorized to charge to Deposit Account No. 50-1165 (XA-10365) any fees under 37 C.F.R. §§ 1.16 and 1.17 that may be required by this paper and to credit any overpayment to that Account. If any extension of time is required in connection with the filing of this paper and has not been separately requested, such extension is hereby requested.

Respectfully submitted,

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